A Hierarchical Active Balancing Architecture for Li-ion Batteries*

Han-Dong Gui[1], Zhiliang Zhang[1], Dong-Jie Gu[1], Yang Yang[1], Zhouyu Lu[1] and Yan-Fei Liu[2], *Fellow, IEEE*

[1]Jiangsu Key Laboratory of New Energy Generation and Power Conversion
Nanjing University of Aeronautics and Astronautics, Nanjing, Jiangsu, P. R. China
[2]Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada, K7L 3N6
{ghdcat, zlzhang, dongjiegu, yyang, luzhouyu} @nuaa.edu.cn and yanfei.liu@queensu.ca

***Abstract*— This paper proposes a hierarchical battery balancing architecture for the series connected lithium-ion batteries. The battery cells are grouped into different packs and the bottom layer is the Adjacent Cell-to-Cell structure consisting of the packs. The top layer is connected to different packs and can deliver the energy from one pack to any other pack bi-directionally, leading to high flexibility. A multi-directional multi-port converter is proposed to serve as the top layer. With the hierarchical architecture, the balanced energy transfer of the cells in different packs can be decoupled, which avoid the repeated charging and discharging during the balancing process. This is beneficial for lengthening the battery lifetime and increasing the State-of-Health (SOH). Moreover, the proposed architecture can lower the current rating of the balancing circuits, which helps decrease the required cost and improve the system efficiency. The experimental results verified the benefits of the proposed architecture.**

***Keywords*----Battery balancing; Cell-to-Cell; multi-port converter; hierarchical layer.**

I. INTRODUCTION

With the wide use and development of electrical vehicles (EV), hybrid electric vehicles (HEV) and energy storage units for renewable energy systems, lithium-ion battery plays a more and more important role because of its advantages such as high energy density, low self-discharge rate, and no memory effect. However, the multiple single cells should be connected in series to meet the voltage requirement of the above applications. Unfortunately, due to the manufacturing inconsistence, environment difference, degradation with the aging and performance characteristics variance, there can be imbalance among the series-connected battery cells, which significantly reduces the energy storage capacity, battery lifetime and safety. Hence, balancing is necessary for the series-connected batteries [1], [2].

Many different balancing methods have been developed and summarized. Among them, the active balancing gains more attention because of the short balancing speed, low energy waste and less heat generation [2]-[15]. From the view of system architecture, it can be categorized into three types: Adjacent Cell-to-Cell (A-C2C) architecture [3]-[5], Direct Cell-to-Cell (D-C2C) architecture [6]-[8] and Cell-to-Pack (C2P) architecture [9]-[11]. For the A-C2C architecture, the balancing circuit has simple structure and low voltage stress of the components. But the adjacent circuits are influenced with each other, leading to complex control and unnecessary energy loss. For the D-C2C architecture, each cell can be balanced independently but only two selected cells can be balanced at the same time, which is not suitable for large number of batteries. For the C2P architecture, different balancing circuits can operate independently but when the target cell is balanced by the mean of discharging, it is also simultaneously charged through the battery pack, which is equivalent to a repeated charging and discharging process for the cell. This phenomenon not only results in energy loss but also harms the state of health (SOH) of the battery. Also, this architecture usually requires the same number of transformers as the number of the cells and the high turns ratio leads to high voltage stress of the semiconductor devices, which results in complex circuit structure, low efficiency and high cost.

In order to solve the above problems, this paper proposes a hierarchical architecture to optimize the balancing performance.

II. PROPOSED HIERARCHICAL ACTIVE BALANCING ARCHITECTURE

Fig. 1 shows the proposed hierarchical architecture, the bottom layer is the A-C2C structure and *n* battery cells are grouped into *m* packs with *p* cells in each pack. In the top layer, each pack is connected to an additional balancing circuit and all the circuits are coupled by a multi-winding transformer. The balanced energy can be exchanged between different packs independently in the top layer with high efficiency.

A. Top Layer

Fig. 2 shows the structure of the top layer. A master battery management system (BMS) calculates the required balancing current of all the balancing circuits in the top and bottom layer. The master BMS directly controls the power flow of the m balancing circuits in the top layer and sends the current reference through CAN interface to the slave BMS in each pack.

The proposed balancing circuits applied in the top layer form a multi-directional multi-port converter. Fig. 3 demonstrates two examples of the possible power flow in the

*This work is supported by Natural Science Foundation of China (51577089) and Lite-On Research Funding.

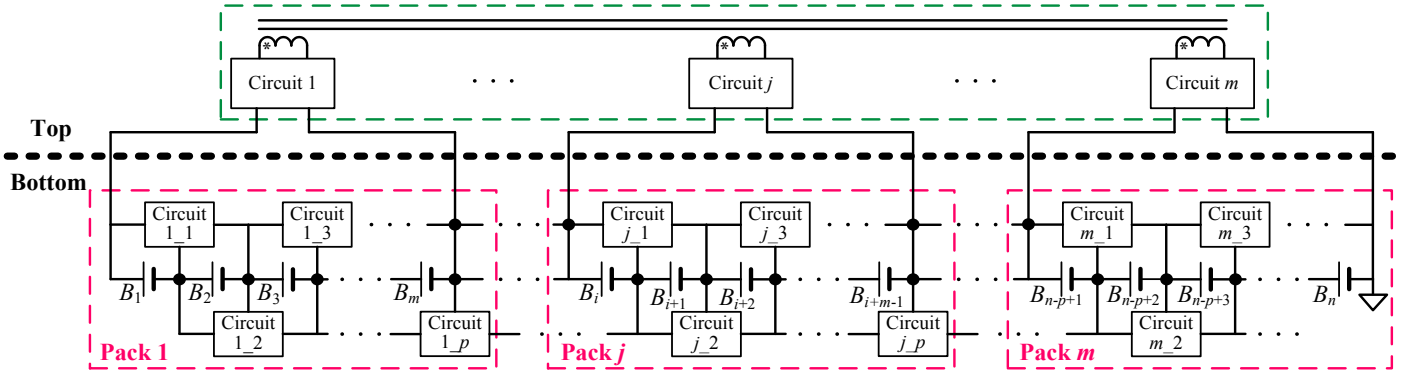


Fig. 1 Proposed hierarchical architecture

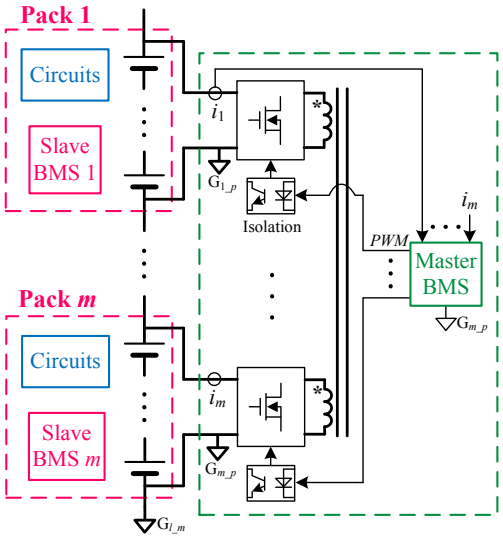


Fig. 2 Structure of top layer

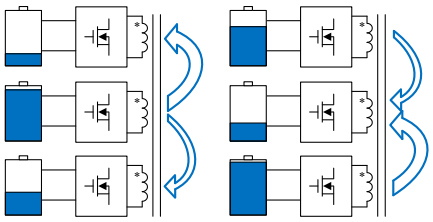


Fig. 3 Two examples of power flow in top layer

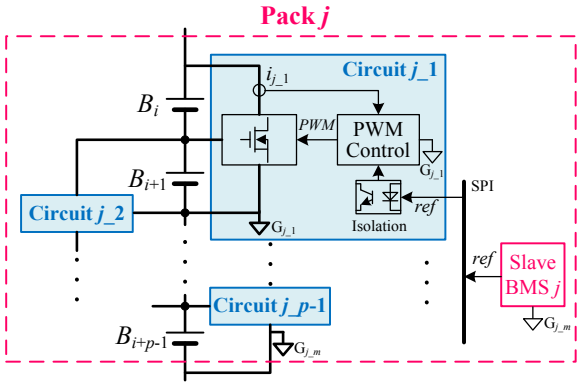


Fig. 4 Structure of bottom layer

converter. It is noted that energy can be delivered by the multi-winding transformer from one pack to any other pack bi-directionally and each pack can serve as both source and load. So this converter owns the advantage of high flexibility of the power flow, which is desired by the balancing system. A multi-port multi-directional converter based on half bridge structure is proposed and applied here and is analyzed in detail in Section III.

B. Bottom Layer

Fig. 4 shows the structure of the bottom layer. The slave BMS detects the operation of the batteries and receives the balancing current reference of each balancing circuit from the master BMS. Each balancing circuit is regulated independently by a local PWM control IC following the balancing current reference sent by the slave BMS through SPI interface.

C. Current Control of the Balancing System

The SOC of *ith* battery cell can be expressed as

$$SOC_i(t) = SOC_i(t_0) + \frac{\int_{t_0}^{t_0+t} \alpha_i I_i(t)dt}{C_i} \tag{1}$$

where $SOC_i(t_0)$ is the initial SOC, α_i is the current acceptance coefficient, C_i is the battery capacity, and $I_i(t)$ is the charging current.

Define K_i equals to C_i/α_i and it represents the variance of battery characteristic and leads to the imbalance. The aim of the control is to introduce a balancing current $I_{b\_i}(t)$ to eliminate the effect of the difference in K_i and keep all the $SOC(t)$ at the same level.

For the top layer, the required balancing current of each circuit can be expressed as

$$\begin{bmatrix} I_{cT\_1}(t) \\ I_{cT\_2}(t) \\ \vdots \\ I_{cT\_m}(t) \end{bmatrix} = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -1 \end{bmatrix} \begin{bmatrix} \frac{\overline{K_1} \cdot \overline{\Delta SOC_1(t)}}{T_b} \\ \frac{\overline{K_2} \cdot \overline{\Delta SOC_2(t)}}{T_b} \\ \vdots \\ \frac{\overline{K_m} \cdot \overline{\Delta SOC_m(t)}}{T_b} \end{bmatrix} \tag{2}$$

where $I_{cT\_j}(t)$ is the required current of jth balancing circuit in the top layer, T_b is the required balancing time, $\overline{\Delta SOC_j(t)}$ is

the difference between the average SOC of the cells in *j*th pack and that of all the cells in the system. $\overline{K_j}$ is defined as

$$\overline{K_j} = \frac{\sum_{i=1}^{p} \frac{C_{j\_i}}{\alpha_{j\_i}}}{p} \tag{3}$$

where C_{j_i} and α_{j_i} is the battery capacity and current acceptance coefficient of *i*th cell in *j*th pack respectively, p is the number of cells in one pack.

For the bottom layer, Fig. 5 shows the power flow of the bottom layer and each dot represents a battery cell. The required current of the *i*th balancing circuit in the bottom layer can be expressed as

$$I_{cB\_i} = \begin{cases} I_{b\_i} & i = 1 \\ I_{b\_i} + I_{cB\_i-1} & i > 1 \end{cases} \tag{4}$$

where I_{cB_i} is the required current of the *i*th balancing circuit, I_{b_i} is the required balancing current of the *i*th cell.

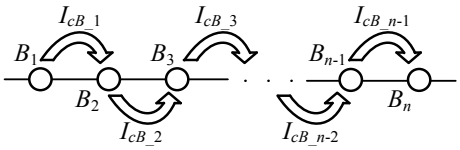


Fig. 5 Power flow in bottom layer

Based on (4), the required balancing current of each circuit can be expressed as

$$\begin{bmatrix} I_{cB\_1}(t) \\ I_{cB\_2}(t) \\ \vdots \\ I_{cB\_n-1}(t) \end{bmatrix} = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ -1 & -1 & \cdots & 0 \\ \vdots & \cdots & \cdots & \vdots \\ -1 & -1 & \cdots & -1 \end{bmatrix} \begin{bmatrix} \frac{K_1 \cdot \Delta SOC_1(t)}{T_b} \\ \frac{K_2 \cdot \Delta SOC_2(t)}{T_b} \\ \vdots \\ \frac{K_{n-1} \cdot \Delta SOC_{n-1}(t)}{T_b} \end{bmatrix} + \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1m} \\ a_{21} & a_{22} & \cdots & a_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ a_{(n-1)1} & a_{(n-1)2} & \cdots & a_{(n-1)m} \end{bmatrix} \begin{bmatrix} I_{cT\_1}(t) \\ I_{cT\_2}(t) \\ \vdots \\ I_{cT\_m}(t) \end{bmatrix} \tag{5}$$

where $\Delta SOC_i(t)$ is the difference between the SOC of *i*th cell and the average SOC of all the cell in the system, the coefficient a_{ij} is

$$a_{ij} = \begin{cases} -1 & (j-1)p < i \le jp \\ 0 & else \end{cases} \tag{6}$$

Thus, from (2) and (5), the required current of all the circuits in both top and bottom layer can be calculated and the BMS in the system is able to regulate the balancing current to complete the balancing process.

D. Advantage of the Proposed Architecture

In the C2P architecture, when a cell is balanced by the means of discharging, part of the balancing current would in turn charge the cell through the battery pack at the same time. This repeated charging and discharging is harmful for the battery SOH. The top layer in the proposed architecture can realize free energy transfer between any two packs through the multi-winding transformer. The battery cells in different packs are totally decoupled and the balancing current would not return to the pack, so the repeated charging and discharging can be avoided and the battery lifetime can be extended. Besides, compared to the C2P architecture with multiple high turns ratio transformers, the number of transformer in the top layer is significantly reduced by selecting proper *m*, so the cost can be decreased and the efficiency can be optimized due to the similar voltage level of each winding.

In the conventional A-C2C balancing system, there is only one way to transfer energy from one cell to another in this system and every two adjacent balancing circuits are influenced by each other. For example, B_1 is the only overcharged cell and the energy stored in B_1 is $E+n\Delta E$, while the energy of all other cells is E. In order to balance the energy of each cell to the same level that equals to $E+\Delta E$, the balancing circuit between B_i and B_i+1 has to transfer $(n\text{-}i)\Delta E$ from B_i to B_i+1. So in order to balance the only overcharged cell, all balancing circuits have to operate at the same time, resulting in considerable energy loss.

In the proposed structure, the top layer supplies an additional energy path among the packs and the cells can be balanced inside each pack independently. So this architecture eliminates the coupled influence between the cells in different packs. Take the aforementioned situation as the example, if the *n* cells are divided into *m* packs, the first pack transfers $(n/l)\Delta E$ to other packs through the top layer. The cells in 1st pack can be balanced inside the pack and the circuits in other packs do not need to operate, which reduces the energy loss of the system.

Furthermore, the current rating of the balancing circuit in the bottom layer can be significantly decreased. Assume that I_{b_i} conforms to uniform distribution

$$I_{b\_i} \sim U(-I_{b\_max}, I_{b\_max}) \tag{7}$$

where I_{b_max} is the maximal possible balancing current of the batteries.

It can be proved that for a series connected battery string with *n* cells, I_{cB_i} conforms to normal distribution

$$I_{cB\_i} \sim N(0, \theta n^2 {I_{b\_max}}^2)$$

$$F(I_{cB\_i}) = \frac{1}{\sqrt{2\pi \cdot \theta n^2 {I_{b\_max}}^2}} e^{-\frac{{I_{cB\_i}}^2}{2\theta n^2 {I_{b\_max}}^2}} \tag{8}$$

where θ is a constant value and $F(I_{cB\_i})$ is the probability density of I_{cB_i}.

From (8), it can be observed that the standard deviation is proportional to *n*, which means that with the same I_{b_max}, larger cell number in a string would introduce wider range of I_{cB_i}.

Fig. 6 shows the graph of $F(I_{cB\_i})$. The blue dotted line is the conventional A-C2C architecture with *n* cells while the red line is the proposed architecture with *n* cells and they are grouped into three packs. In order to meet the balancing requirement in 90% random cases, the current rating of the balancing circuit should be designed at point *A* for the blue line and *B* for the red line, and *A* is about three times larger than *B*. So the current rating of the balancing circuit in the bottom layer can be reduced to one-third by applying the proposed architecture, which is essential for decreasing cost and improving efficiency.

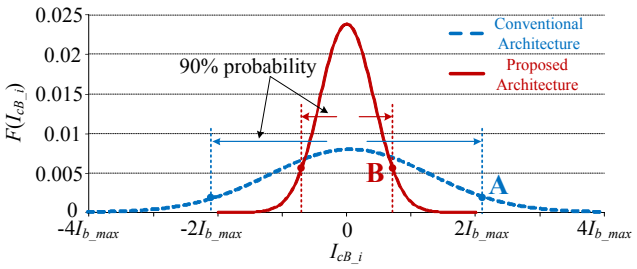


Fig. 6 Probability density of required balancing current

III. Balancing Circuits in the Proposed Architecture

A. Proposed Multi-directional Multi-port Converter in Top Layer

In order to realize the aforementioned function of the balancing circuit in the top layer, a multi-directional multi-port converter based on half bridge structure is proposed.

Fig. 7 illustrates the topology of the converter. Each battery pack is connected to a half bridge as the balancing circuit shown in Fig. 1. T is a multi-winding transformer and L_{rj} is the leakage inductance that serves as the energy transfer element. Phase Shift Modulation is applied to control the value and direction of the power flow in different circuits.

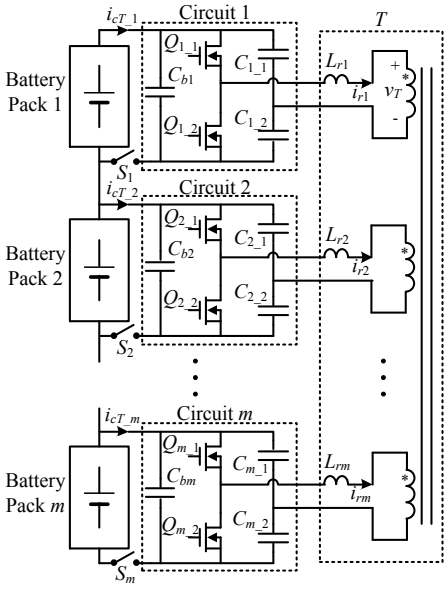


Fig. 7 Topology of the proposed converter

In the proposed converter, each half bridge generates a square wave voltage and its amplitude equals to the half of the voltage of the battery pack. Fig. 8 presents the equivalent model of the proposed converter.

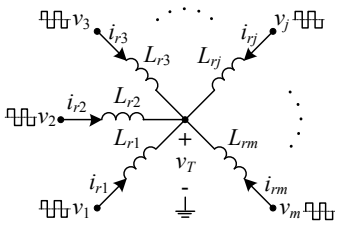


Fig. 8 Equivalent model of the proposed converter

Assume that each battery pack owns the same voltage V_b and each leakage inductance is the same as L_r. Fig. 9 shows the key waveforms of the proposed converter when m=3. The current of different circuits I_{cT_j} equals to the average value of the shaded area.

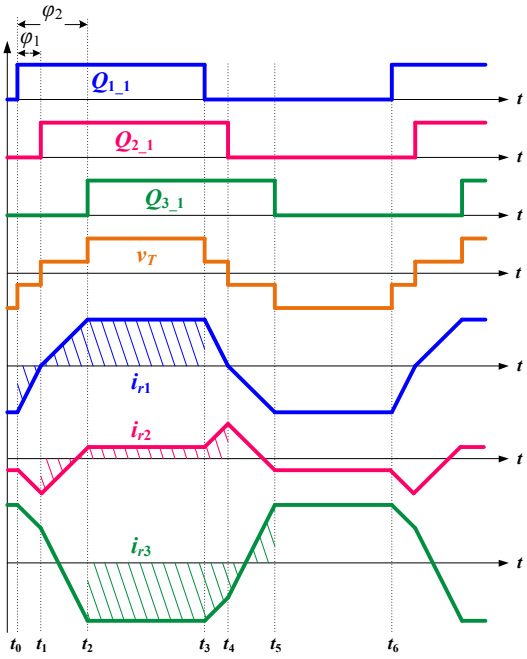


Fig. 9 Key waveforms of the proposed converter with m=3

The peak to peak value of the current on leakage inductance ΔI_{rj} is given by

$$\begin{bmatrix} \Delta I_{r1} \\ \Delta I_{r2} \\ \Delta I_{r3} \\ \vdots \\ \Delta I_{r(m-1)} \\ \Delta I_{rm} \end{bmatrix} = \frac{V_b}{4\pi L_r \cdot f_{sT}} M \begin{bmatrix} \varphi_1 \\ \varphi_2 - \varphi_1 \\ \varphi_3 - \varphi_2 \\ \vdots \\ \varphi_{m-2} - \varphi_{m-3} \\ \varphi_{m-1} - \varphi_{m-2} \end{bmatrix} \tag{9}$$

$$M = \begin{bmatrix} \frac{2(m-1)}{m} & \frac{2(m-2)}{m} & \cdots & \frac{4}{m} & \frac{2}{m} \\ \frac{2}{m} & \frac{2(m-2)}{m} & \cdots & \frac{4}{m} & \frac{2}{m} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{2}{m} & \frac{4}{m} & \cdots & \frac{2(m-2)}{m} & \frac{2}{m} \\ \frac{2}{m} & \frac{4}{m} & \cdots & \frac{2(m-2)}{m} & \frac{2(m-1)}{m} \end{bmatrix} \tag{10}$$

where φ_j is the phase shift angle between Circuit j+1 and Circuit 1, f_{sT} is the switching frequency.

Based on (9), the relationship between the phase shift angles and the current of each circuit can be derived as (11). Therefore, the balancing current in the top layer can be regulated by controlling the phase shift angles.

$$\begin{bmatrix} I_{cT\_1} \\ I_{cT\_2} \\ I_{cT\_3} \\ \vdots \\ I_{cT\_m-1} \\ I_{cT\_m} \end{bmatrix} = \begin{bmatrix} -\frac{\Delta I_{r1}}{4} \\ -\frac{\Delta I_{r2}}{4} \\ -\frac{\Delta I_{r3}}{4} \\ \vdots \\ -\frac{\Delta I_{r(m-1)}}{4} \\ -\frac{\Delta I_{rm}}{4} \end{bmatrix} + \frac{V_b}{32\pi^2 L_r \cdot f_{sT}} \left(M \begin{bmatrix} \varphi_1^2 \\ \varphi_2^2 \\ \varphi_3^2 \\ \vdots \\ \varphi_{m-2}^2 \\ \varphi_{m-1}^2 \end{bmatrix} + diag\left(M \begin{bmatrix} \varphi_1 & & & \\ & \varphi_2-\varphi_1 & & \\ & & \ddots & \\ & & & \varphi_{m-1}-\varphi_{m-2} \end{bmatrix} \times \right. \right. \tag{11}$$

$$\left. \left. \begin{bmatrix} \pi-\varphi_1 & 0 & \varphi_2-\varphi_1 & \cdots & \varphi_{m-2}-\varphi_{m-3} & \varphi_{m-1}-\varphi_{m-2} \\ \pi-\varphi_2 & \pi+\varphi_1-\varphi_2 & 0 & \cdots & \varphi_{m-3}-\varphi_{m-4} & \varphi_{m-2}-\varphi_{m-3} \\ \pi-\varphi_3 & \pi+\varphi_1-\varphi_3 & \pi+\varphi_2-\varphi_3 & \cdots & \varphi_{m-4}-\varphi_{m-5} & \varphi_{m-3}-\varphi_{m-4} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \pi-\varphi_{m-2} & \pi+\varphi_1-\varphi_{m-2} & \pi+\varphi_2-\varphi_{m-2} & \cdots & 0 & \varphi_2-\varphi_1 \\ \pi-\varphi_{m-1} & \pi+\varphi_1-\varphi_{m-1} & \pi+\varphi_2-\varphi_{m-1} & \cdots & \pi+\varphi_{m-2}-\varphi_{m-1} & 0 \end{bmatrix} \right)$$

B. Buck Boost Converter in Bottom Layer

The conventional buck boost converter is applied to serve as the balancing circuit in the bottom layer because of its simple structure and the ability to control the operating current bi-directionally. Fig. 10 illustrates its topology.

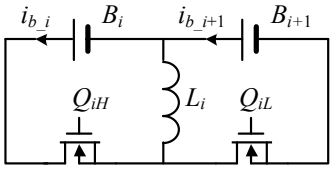


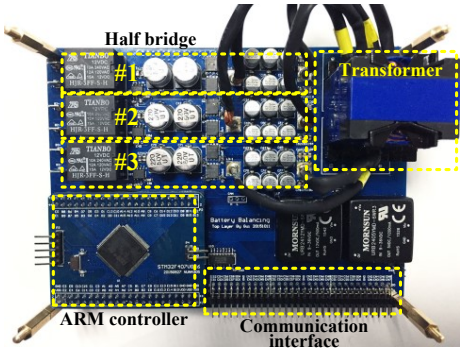
Fig. 10 Topology of buck boost converter in bottom layer

IV. Experimental Results and Discussion

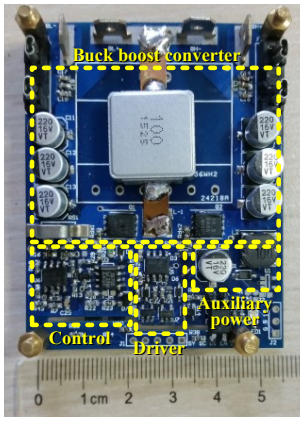
To verify the analysis of the proposed architecture, a hardware platform is built. In the system, 24 battery cells are connected in series and the rated capacity of each cell is 200 Ah. They are grouped into 3 packs with 8 cells in each pack. The maximal charging/discharging current of the batteries is 200 A. The maximal variance of different battery characteristic is 5%. The current rating of the balancing circuit in the bottom layer is set as 10 A. According to (8), 98% imbalance cases can be included and well solved. Similarly, the current rating of the balancing circuit in the top layer is 3.6 A. Table I lists the parameters of the balancing circuits in the top and bottom layer. Fig. 11 shows the photos of the prototype.

Table I Circuit parameters of converters in top and bottom layer

	Top layer	Bottom layer
Input/output voltage	24~36 V	3.2~4.2 V
Output power	130 W	42 W
Balancing current	-3.6~3.6 A	-10~10 A
Switching frequency	100 kHz	120 kHz
Inductance	1 μH (L_{rj})	10 μH (L_i)
MOSFETs	BSC039N06NS	SiR416DP
Controller	STM32F407VG	UCC35705



(a) Top layer



(b) Bottom layer

Fig. 11 Photo of prototype

Fig. 12 and Fig. 13 show the experimental waveform of the balancing current in the top and bottom layer. In Fig. 12, the balancing current of the three packs is 3.6 A, -1 A and -2.6 A respectively. In Fig. 13, the balancing current of the two cells is 10 A and -10 A. Thus, both the balancing circuits in the top and bottom layer can operate properly, which verifies the effectiveness of the proposed architecture.

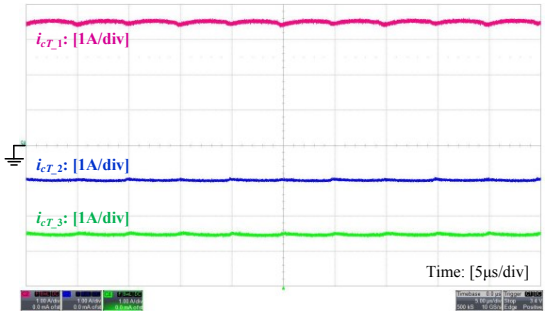


Fig. 12 Balancing current in top layer

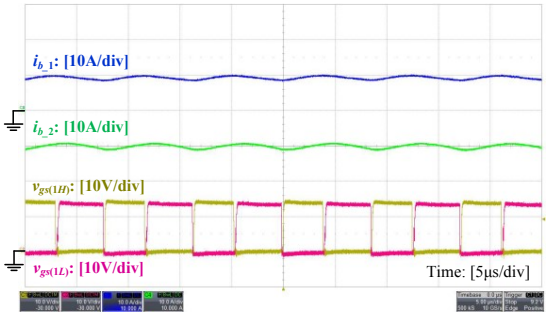


Fig. 13 Balancing current in bottom layer

Fig. 14 illustrates the current rating density of the balancing circuit, which is the ratio of the balancing current rating and the battery capacity. Compared to other literature, the minimal and maximal reduction of the current rating is 50% and 90% respectively by the proposed architecture. So the system applied with the proposed architecture needs far less current than other architecture when the same battery is balanced.

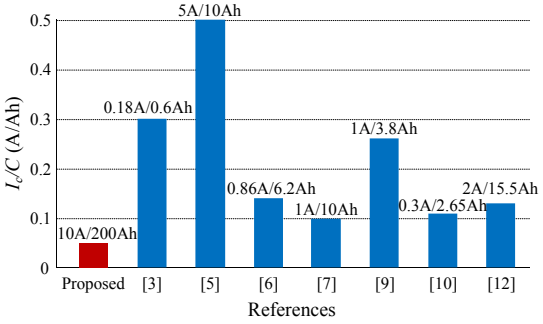


Fig. 14 Comparison of current rating density in different architecture

V. Conclusion

In this paper, a hierarchical architecture is proposed to improve the performance of the balancing system for series connected batteries. In the proposed architecture, the batteries in the bottom layer are applied with the Adjacent Cell-to-Cell structure and they are grouped into different packs. A multi-directional multi-port converter is proposed to form the top layer and it can deliver the energy from one pack to any other pack bi-directionally. The top layer decouples the battery cells in different packs and avoids the repeated charging and discharging problem in the Cell-to-Pack architecture. Thus the battery lifetime can be extended. Moreover, the proposed architecture can reduce the required current rating of the balancing circuits. According to the experimental results, the effectiveness of the balancing circuits in the proposed architecture is validated and the current rating of the balancing circuits with the proposed architecture is much lower than that with other architecture.

References

[1] Z. Zhang, Y. Y. Cai, Y. Zhang, D. J. Gui and Y. F. Liu, "A distributed architecture based on micro-bank modules with self-reconfiguration control to improve the energy efficiency in the battery energy storage system," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 304-317, Jan. 2016.

[2] J. G.-Lozano and E. R. Cadaval, "Battery equalization active methods," *J. Power Sources*, vol. 246, pp. 934–949, 2014.

[3] Y. Yuanmao, K. W. E. Cheng and Y. P. B. Yeung, "Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3234–3242, Jul. 2012.

[4] M. Uno and K. Tanaka, "Single-switch cell voltage equalizer using multistacked buck–boost converters operating in discontinuous conduction mode for series-connected energy storage cells," *IEEE Trans. Veh. Technol.*, vol. 60, no. 8, pp. 3635–3645, Oct. 2011.

[5] T. Phung, A. Collet and J.-C. Crebier, "An optimized topology for next-to-next balancing of series-connected lithium-ion cells," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4603–4613, Sep. 2014.

[6] Y. Shang, C. Zhang, N. Cui and J. M. Guerrero, "A cell-to-cell battery equalizer with zero-current switching and zero-voltage gap based on quasi-resonant LC converter and boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3731-3747, Jul. 2015.

[7] F. Baronti, G. Fantechi, R. Roncella and R. Saletti, "High-efficiency digitally controlled charge equalizer for series-connected cells based on switching converter and super-capacitor," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1139–1147, May. 2013.

[8] F. Mestrallet, L. Kerachev, J. C. Crebier and A. Collet, "Multiphase interleaved converter for lithium battery active balancing," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2874–2881, Jun. 2014.

[9] C.-S. Lim, K.-J. Lee, N.-J. Ku, D.-S. Hyun and R.-Y. Kim, "A modularized equalization method based on magnetizing energy for a series-connected lithium-ion battery string," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1791–1799, Apr. 2014.

[10] A. M. Imtiaz and F. H. Khan, "Time shared flyback converter' based regenerative cell balancing technique for series connected Li-ion battery strings," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5960–5975, Dec. 2013.

[11] M. Einhorn, W. Guertlschmid, T. Blochberger, R. Kumpusch, R. Permann, F. V. Conte, C. Kral and J. Fleig, "A current equalization method for serially connected battery cells using a single power converter for each cell," *IEEE Trans. Veh. Technol.*, vol. 60, no. 9, pp. 4227–4237, Nov. 2011.

[12] M. Y. Kim, J. H. Kim and G. W. Moon, "Center-cell concentration structure of a cell-to-cell balancing circuit with a reduced number of switches", *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5285–5297, Oct. 2014.

[13] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.

[14] H. Chen, L. Zhang and Y. Han, "System-theoretic analysis of a class of battery equalization systems: mathematical modeling and performance evaluation," *IEEE Trans. Veh. Technol.*, vol. 64, no. 4, pp. 1445–1457, Apr. 2015.

[15] S. Li, C. Mi, and M. Zhang, "A high-efficiency active battery-balancing circuit using multiwinding transformer," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 198–207, Jan. 2013.